an array of rows and columns of volatile memory cells;

addressing circuitry for providing access to selected ones of said memory cells;

master read/write circuitry for reading and writing data into said selected ones of said cells;

first slave circuitry for storing data for exchange with said master read/write circuitry;

second slave circuitry for storing data for exchange with said master read/write circuitry; and

control circuitry for controlling exchange of data between said master read/write circuitry and said first and second slave circuitry, said control circuitry operable during a move operation to:

control the sensing by said master read/write circuitry of data from a said row in said array selected by said addressing circuitry;

control the transfer of said data from said master read/write circuitry to a selected one of said first and second slave circuitry;and

control the writing of said data through said master read/write circuitry to a second said row in said array selected by said addressing circuitry.

In Claim 2, line 1, after "is" insert -- further --.

7. (Amended) A memory system comprising:

an array of memory cells arranged in rows and columns, each said row associated with a conductive wordline and each said column associated with a conductive bitline;

a row decoder coupled to said wordlines;

a bank of master sense amplifiers coupled to said bitlines;

a plurality of banks of slave sense amplifiers coupled to said master sense amplifiers;

a column decoder coupled to each of the plurality of banks of slave sense amplifiers; and

control circuitry coupled to said row decoder, said bank of master sense amplifiers and said banks of slave sense amplifiers, said control circuitry including mode control circuitry coupled to said row decoder and said master sense amplifiers and multiplexer control circuitry coupled to said mode control circuitry and said plurality of banks of slave sense amplifiers, said control circuitry operable during a move operation to:

control the sensing by said master sense amplifiers of data from a said row in said array selected by said row decoder;

control the transfer of said data from said master sense amplifiers to a selected one of said banks of slave sense amplifiers;

control the writing of said data through said master sense amplifiers to a second said row in said array selected by said row decoder.

Please cancel Claim 8.

In Claim 9, lines 3, 6, 9, and 12, delete "the".

In Claim 11, lines 3, 6, 9, and 12, delete "the".

Please cancel Claim 13.

14. (Amended) A memory system comprising: [The memory system of Claim 8 wherein said control circuitry is operable during a block move operation to:]

an array of memory cells arranged in rows and columns, each said row associated with a conductive wordline and each said column associated with a conductive bitline;

a row decoder coupled to said wordlines;

a bank of master sense amplifiers coupled to said bitlines;

a plurality of banks of slave sense amplifiers coupled to said master sense amplifiers;

a column decoder coupled to each of the plurality of banks of slave sense amplifiers; and

said control circuitry including mode control circuitry coupled to said row decoder and said master sense amplifiers and multiplexer control circuitry coupled to said mode control circuitry and said first and second banks of slave sense amplifiers, said control circuitry operable during a block move operation to:

control the sensing by said master sense amplifiers of data from a said row in said array selected by said row decoder;

control the transfer of said data from said master sense amplifiers to a selected one of said banks of slave sense amplifiers;

control the shifting of said data from a first set of slave sense amplifiers to a second set of slave sense amplifiers within said selected bank of slave amplifiers; and

control the writing of said data through said master sense amplifiers to ones of said cells along said selected said row associated with said bitlines coupled to said second set of slave sense amplifiers.

13. (Amended) A memory comprising:

an array of dynamic random access memory cells arranged in rows and columns, each said row including a conductive wordline and each said column including a conductive bitline;

row decoder circuitry coupled to said wordlines for selecting a said row in response to a row address;

master sense amplifier circuitry coupled to said bitlines for reading and writing data to ones of said cells along a selected said row;

column decoder circuitry coupled to a data bus;

first latching circuitry coupled to said sense amplifier circuitry by a first local bus and to said column decoder by a second local bus for latching data being exchanged between said sense amplifier circuitry and said column decoder;

second latching circuitry coupled to said sense amplifier circuitry by said first local bus and to said column decoder by said second local bus for latching data being exchanged between said sense amplifier circuitry and said column decoder; and

control circuitry for [controlling said first and second latching circuitry said control circuitry alternately latching data being exchanged between said sense amplifier circuitry and said column decoder in said first latching circuitry and said second latching circuitry]:

causing said master sense amplifier circuitry to sense data from a said row selected by said row decoder;

transferring said data from said master sense amplifier circuitry to said first slave sense amplifier circuitry;

writing said data from said first slave sense amplifiers to said second row selected by said row decoder;

causing said master sense amplifier circuitry to sense data from a third said row selected by said row decoder;

transferring said data from said master sense amplifier circuitry to said second slave sense amplifier circuitry;and

writing said data from said second slave sense amplifiers to a fourth said row selected by said row decoder.

Please cancel Claims 19-21.

22. (Amended) A method of performing a block transfer within a memory including an array of memory cells arranged in rows and columns, each said row associated with a conductive wordline and each said column associated with a conductive bitline, comprising the steps of:

selecting a row in the array;

sensing the bitlines of the array to read data stored in the cells of the selected row with a bank of master sense amplifiers;

latching the data read from the cells of the selected row in a bank of slave sense amplifiers;

writing the data stored in the slave sense amplifiers through the master sense amplifiers to [other] different cells in the array.

18 23. (Amended) The method of Claim 17 22 wherein said step of writing comprises the [step] substeps of:

shifting the data within the slave sense amplifiers from a first selected set of said slave amplifiers to a second selected set of said slave amplifiers; and

writing the data from the second set of slave amplifiers to the different [other] cells in the selected row in the array.

19 24. (Amended) The method of Claim 17 22 wherein said step of writing comprises the step of writing data from the slave sense amplifiers to cells of a different [another] row in the array.

REMARKS

In the Office Action mailed March 23, 1995, Claims 1-24 stand rejected. In view of the above amendments, Applicant respectfully requests reconsideration.

I. The Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 8, 11-14 and 22-24 stand rejected under 35 U.S.C.